AMENDMENTS TO THE CLAIMS

1-32. (Canceled)

33. (Currently Amended) A method of operating an integrated circuit memory device, said method comprising:

providing a layer of metalized traces including a plurality of I/O traces;

including within said layer of metalized traces a plurality of non-I/O traces, and disposing at least one non-I/O trace between every two I/O traces;

introducing a plurality of I/O signals, each of said I/O signals exhibiting a transient portion and a non-transient portion, onto said plurality of I/O traces respectively;

introducing a plurality of non-I/O signals, each of said non-I/O signals exhibiting a transient portion and a non-transient portion, onto said plurality of non-I/O traces respectively[[,]]; and

applying said I/O signals and said non-I/O signals such that said I/O signal transient portions occur only during non-transient portions of said non-I/O signals.

34. (Canceled)

35. (Currently Amended) A method of operating an integrated circuit memory device comprising:

providing an integrated circuit including a substrate assembly and a layer of metallic traces disposed in substantially parallel spaced relation over said substrate assembly;

providing among said layer of metallic traces a first plurality of I/O traces interspersed with a second plurality of non-I/O traces such that at least one non-I/O trace is disposed between every two said I/O traces;

during a first time period, introducing a plurality of first electrical signals, each including a transient portion followed by a non-transient portion, one onto each of said non-I/O traces respectively, and allowing each of said plurality of first electrical signals to reach said non-transient portion; and

during a second time period, subsequent to said first time period, introducing a plurality of second electrical signals, each including a transient portion followed by a non-transient portion, one onto each of said plurality of I/O traces respectively such that said transient portion of said second electrical signals occurs exclusively during said non-transient portion of said first electrical signals.

36. (Previously Presented) A method as in claim 35 further comprising providing a plurality of additional layers of metalization, wherein said plurality of I/O traces is spaced farther from said substrate than any of said additional layers.

37-54. (Canceled)